

What is claimed is:

- 1 1. A fault tolerant computer comprising:
  - 2 a plurality of CPU (Central Processing Unit) modules
  - 3 processing the same instruction string while maintaining clock
  - 4 synchronization;
  - 5 a plurality of I/O modules each having a plurality of device
  - 6 controllers each executing input/output control processing for
  - 7 a device; and
  - 8 a transaction synchronization controller, provided in
  - 9 each of said device controllers, that checks if sequences of
  - 10 I/O transactions issued from said plurality of CPU modules match
  - 11 and, if the sequences match, judges that an
  - 12 out-of-synchronization condition is not caused.
- 1 2. The fault tolerant computer according to claim 1 wherein
  - 2 said transaction synchronization controller comprises:
    - 3 timer means for measuring a predetermined time; and
    - 4 comparison means for checking if the sequences of I/O
    - 5 transactions, issued from the plurality of CPU modules, match
    - 6 on a device controller basis while waiting for the predetermined
    - 7 time.
- 1 3. The fault tolerant computer according to claim 2 wherein
  - 2 said transaction synchronization controller further comprises
  - 3 an output controller that outputs said I/O transactions to said
  - 4 device controller when said sequences match.
- 1 4. The fault tolerant computer according to claim 3 wherein,

2 when the I/O transactions from the CPU modules match, said output  
3 controller outputs the matching I/O transactions to said device  
4 controller, one at a time.

1 5. The fault tolerant computer according to claim 2 wherein,  
2 when the sequences do not match within the predetermined time  
3 or when the sequences of I/O transactions differ, said output  
4 controller outputs a failure notification.

1 6. The fault tolerant computer according to claim 2, further  
2 comprising a plurality of storage means in which the I/O  
3 transactions issued from said plurality of CPU modules are  
4 stored.

1 7. The fault tolerant computer according to claim 2 wherein  
2 said transaction synchronization controller further comprises  
3 selection circuits that select between said plurality of storage  
4 means and said CPU modules as a source from which I/O transactions  
5 to be sent to said comparison means are received.

1 8. A transaction synchronization control method for use in a  
2 fault tolerant computer, said method comprising:  
3 a first step of sending a plurality of, and the same, I/O  
4 transactions from a plurality of CPU modules, which process the  
5 same instruction string while maintaining clock synchronization,  
6 to an I/O module; and  
7 a second step of checking if sequences of the received  
8 I/O transactions match in each of a plurality of device

9 controllers provided in said I/O module and, if the sequences  
10 match, judging that an out-of-synchronization condition is not  
11 caused.

1 9. The transaction synchronization control method according  
2 to claim 8 wherein said second step checks if the sequences of  
3 I/O transactions match while waiting for a predetermined time.

1 10. The transaction synchronization control method according  
2 to claim 9, further comprising a third step of outputting the  
3 I/O transactions to said device controller when the sequences  
4 match.

1 11. The transaction synchronization control method according  
2 to claim 9 wherein, for each device controller, said first step  
3 stores the I/O transactions issued from said plurality of CPU  
4 modules into a plurality of storage means and  
5 wherein said second step sends the I/O transactions,  
6 received from the CPU modules, to comparison means for use in  
7 comparing the I/O transactions, checks if the predetermined time  
8 has elapsed if the I/O transactions do not match, and judges  
9 that an out-of-synchronization condition is not caused if the  
10 predetermined time has not yet elapsed.

1 12. The transaction synchronization control method according  
2 to claim 11 wherein, when the received I/O transactions match,  
3 the matching I/O transactions are output to said device  
4 controller, one at a time.

1 13. The transaction synchronization control method according  
2 to claim 9, further comprising the step of outputting a failure  
3 notification when the sequences do not match within the  
4 predetermined time.

1 14. The transaction synchronization control method according  
2 to claim 11, further comprising the step of selecting between  
3 said plurality of storage means and said CPU modules as a source  
4 when a new I/O transaction is sent to said comparison means.

1 15. The transaction synchronization control method according  
2 to claim 14 wherein, when the storage means do not contain  
3 effective data, said step of selecting between said plurality  
4 of storage means and said CPU modules switches the source to  
5 the CPU modules.

1 16. A transaction synchronization control program product for  
2 use in a fault tolerant computer in which the same instruction  
3 string is processed by a plurality of CPU modules while  
4 maintaining clock synchronization, said program product  
5 comprising:

6 a first step of sending a plurality of, and the same, I/O  
7 transactions from the plurality of CPU modules to an I/O module;  
8 and

9 a second step of checking if sequences of the received  
10 I/O transactions match in each of a plurality of device  
11 controllers provided in said I/O module and, if the sequences

12 match, judging that an out-of-synchronization condition is not  
13 caused.

1 17. The transaction synchronization control program product  
2 according to claim 16 wherein said second step checks if the  
3 sequences of I/O transactions match while waiting for a  
4 predetermined time.

1 18. The transaction synchronization control program product  
2 according to claim 17, further comprising a third step of  
3 outputting the I/O transactions to said device controller when  
4 the sequences match.

1 19. The transaction synchronization control program product  
2 according to claim 16, further comprising the step of outputting  
3 a failure notification when the sequences do not match within  
4 the predetermined time or when the sequences of I/O transactions  
5 differ.

1 20. The transaction synchronization control program product  
2 according to claim 17

3                   wherein, for each device controller, said first  
4 step comprises the step of storing the I/O transactions, issued  
5 from said plurality of CPU modules, into a plurality of storage  
6 means and

7                   wherein said second step comprises the steps of sending  
8 the I/O transactions received from the CPU modules to comparison  
9 means and comparing the I/O transactions; checking if the

10 predetermined time has elapsed if the I/O transactions do not  
11 match; and judging that an out-of-synchronization condition is  
12 not caused when the predetermined time has not yet elapsed.